LISTING OF CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original) A PMOS device having a drain junction breakdown point and a maximum impact ionization point, and including:

a gate;

a body; and

a drain formed in the body, wherein at least one of the drain junction breakdown point and the maximum impact ionization point is located within at least one of the body and the drain so as to reduce any drain breakdown voltage walk-in exhibited by the device below a predetermined value.

2. (original) The PMOS device of claim 1, wherein both the drain junction breakdown point and the maximum impact ionization point are located sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

3. (original) The PMOS device of claim 2, wherein both the drain junction breakdown point and the maximum impact ionization point are located sufficiently far from the gate that any drain breakdown voltage walk-in exhibited by the device has absolute magnitude not greater than two volts.

4. (original) The PMOS device of claim 1, wherein the PMOS device is a high voltage power transistor, the high voltage power transistor includes an extended drain region formed in the body, the extended drain region includes the drain, a deep drain implant, and a lightly doped drain implant between the deep drain implant and the gate, at least a portion of the lightly doped drain implant is located between the drain and the gate, and at least a portion of the deep drain implant is located below the drain.

5. (original) The PMOS device of claim 4, wherein both the drain junction breakdown point and the maximum impact ionization point are located sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

6. (original) The PMOS device of claim 4, wherein both the drain junction breakdown point and the maximum impact ionization point have been located sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value, by controlling an implant dose employed to produce the lightly doped drain implant.

7. (original) The PMOS device of claim 6, wherein the device has been manufactured in accordance with a BiCMOS process, and the implant dose is much less than 2.23×10^{12} ions/cm^2 .

8. (original) The PMOS device of claim 7, wherein the implant dose is at least substantially equal to 1.15×10^{12} ions/cm^2.

9. (original) The PMOS device of claim 1, wherein the drain junction breakdown point is located sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

10. (original) The PMOS device of claim 1, wherein the maximum impact ionization point is located sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

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